Application No.: 10/709,041 Docket No.: 21806-00158-US

REMARKS

Claims 1-15 are pending in the present application. Figures 1-3 and claims 1, 7, 9, 11, 12, 13 and 14 have been amended by way of the present amendment. Reconsideration is respectfully requested.

In the outstanding Office Action, Figures 1-3 have been indicated as needing a legend, such as Prior Art; claims 9, 11, 13 and 14 have been objected to due to informalities; claims 9 and 11 were rejected under 35 U.S.C. 112, 2nd paragraph; claims 1-6 and 13-15 were rejected under 35 U.S.C. Section 103(a) as unpatentable over the Applicant's Prior Art Figure 2B (APAF) in view of U.S. Patent Publication No. 2002/0122280 (Ker et al. I); claims 7, 8 and 10-12 were rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of U.S. Patent No. 6,566,715 (Ker et al. II); and claim 9 was rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of Ker et al. II as applied to claim 7 above, and further in view of Ker et al. I.

Drawing Objections

Figures 1-3 were indicated to need a legend such as Prior Art. In response to the rejection, Figures 1-3 have been amended to include the legend "Background Art." Replacement sheets for Figures 1-3 including the legend "Background Art" are filed herewith. Applicants respectfully submit that the amendments raise no question of new matter. As a result, Applicants request that the outstanding objection be withdrawn.

Claim Objections

Claims 9 and 12-14 have been objected to due to informalities. Claims 9 and 12-14 have been amended in accordance with the suggestions contained in the outstanding Office Action. Applicants respectfully submit that the amendments raise no question of new matter. As a result, Applicants request that the outstanding objections be withdrawn.

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35 USC Section 112 Rejections

Claims 9 and 11 were rejected under 35 U.S.C. 112, 2nd paragraph. Claims 9 and 11 have been amended in accordance with the suggestions contained in the outstanding Office Action. In addition, support for the amendment is shown at least in Figure 4 of the application. Applicants respectfully submit that the amendments raise no question of new matter. As a result, Applicants request that the outstanding rejections be withdrawn.

35 USC Section 103 Rejections

Claims 1-6 and 13-15 were rejected under 35 U.S.C. Section 103(a) as unpatentable over APAF in view of Ker et al. I. Applicants respectfully traverse the rejection.

Independent claims 1, 7 and 13 have been amended to clarify the invention. In particular, claim 1 has been amended to recite:

> a substrate having first, second and third wells formed in said substrate, and separated by shallow well isolation regions, ~~said first and third wells connected along a bottom thereof with a conductive band region~~ generally separating the bottom of said second well from said substrate with a segmented conductive band;
>
> a source and drain region in said second well forming an FET, said drain being connected to an I/O pad for protecting said pad against an ESD event; and
>
> a path of substrate material extending through an opening in said conductive band region, ~~to increase~~ increasing the substrate resistance in the path of the current which flows through said I/O pad to a substrate contact and drain during an ESD event and electrically connecting the second well to the substrate,
>
> wherein the first and third wells are completely isolated from the drain and source, and the substrate contact is located outside the first and third wells.

Claims 7 and 13 have been amended in a similar manner. Support for the amendment is provided at least at paragraph [0027] and shown in FIG. 4 of the published application. Therefore, it is respectfully submitted that the amendment raise no question of new matter.

APAF discloses the implementation of an ESD NMOSFET in a triple well CMOS architecture.[1] In particular, the APAF discloses an additional N-Band **40** that constitutes an n-type doped region which in combination with the N-Wells **37** and **38** isolates the P-well **31** from the substrate **41**.[2] As can be seen from FIG. 2B of the specification, the triple well architecture of the background art is similar to the dual well architecture, *with the exception of the additional N-Band 40, and N-wells 37 and 38*.[3] N-well **37** and **38** are connected in the embodiment shown to a source of positive potential VDD.[4] Additionally, two other isolation regions **33** and **34** are provided to provide isolation for the N-wells **37** and **38**.[5]

However, the APAF nowhere discloses, as recited in independent claim 1:

> a substrate having first, second and third wells formed in said substrate, and separated by shallow well isolation regions, generally separating the bottom of said second well from said substrate *with a segmented conductive band*;
>
> a source and drain region in said second well forming an FET, said drain being connected to an I/O pad for protecting said pad against an ESD event; and
>
> a path of substrate material extending through an opening in said conductive band region, increasing the substrate resistance in the path of the current which flows through said I/O pad to a substrate contact and drain during an ESD event and *electrically connecting the second well to the substrate*,
>
> wherein the first and third wells are completely isolated from the drain and source, *and the substrate contact is located outside the first and third wells* (emphasis added).

[1] *Id.* at page 2, paragraph [0024], lines 1-2.
[2] *Id.* at page 2, paragraph [0024], lines 2-5.
[3] *Id.* at page 2, paragraph [0024], lines 5-8.
[4] *Id.* at page 2, paragraph [0024], lines 8-10.
[5] *Id.* at page 2, paragraph [0024], lines 10-12.

That is, the APAF nowhere discloses either "a segmented conductive band" nor "electrically connecting the second well to neither the substrate "nor" the substrate contact is located outside the first and third wells." Therefore, the APAF does not disclose the claimed invention.

In addition, the outstanding Office Action acknowledges deficiencies in the APAF and attempts to overcome these deficiencies by combining the APAF with Ker et al. I. However, Ker et al. I cannot overcome all of the deficiencies of the APAF as will be discussed below.

Ker et al. I discloses an electrostatic discharge (ESD) protection component with a deep-N-well structure in CMOS technology.[6] In particular, Ker et al. I discloses an N-type Silicon Controlled Rectifier (NSCR) device with a deep N-well, as shown in FIG. 5. Further, Ker et al. I discloses that there are three nodes in the NSCR structure: (1) the anode; (2) the cathode; and (3) the control gate (VGN).[7]

In addition, Ker et al. I discloses that the PNPN structure of the NSCR is composed of the P+ diffusion **52**, the N-well **42**, the P-well **40** and the N+ diffusion **46**.[8] The P+ diffusion **52** is used as the anode of the NSCR device and an NMOS is inserted into the P-well **40**.[9] The drain of the NMOS is formed by the N+ diffusion **44** at the P-N junction of the P-well **40** and the N-well **42**.[10] The source of the NMOS is formed by the N+diffusion **46**, used as the cathode of the NMOS device.[11]

Furthermore, Kerr et al. I discloses that in this modified device structure, the P-well 40 of the NSCR device is partially connected to the common P-substrate **30**.[12] But the two deep N-well regions **3201** and **3202** are placed closer to limit the connection region of the P-well 40 and the P-substrate **30**, thereby increasing the equivalent resistance between them.[13] The deep N-well

[6] Ker et al. I at ABSTRACT.
[7] *Id.* at page 3, paragraph [0047], lines 2-4.
[8] *Id.* at page 3, paragraph [0047], lines 4-6.
[9] *Id.* at page 3, paragraph [0047], lines 6-8.
[10] *Id.* at page 3, paragraph [0047], lines 8-10.
[11] *Id.* at page 3, paragraph [0047], lines 10-11.
[12] *Id.* at page 3, paragraph [0047], lines 11-13.
[13] *Id.* at page 3, paragraph [0047], lines 14-17.

3201 is connected to N-well 60, the deep N-well 3202 is connected to N-well 42. [14] When proper voltage is applied to the control gate VGN, the trigger current from the NMOS into the P-well 40 turns on the NSCR more quickly within the limited connection region. [15]

However, Ker et al. I nowhere discloses, as recited in independent claims 1, 7 and 13:

> wherein the *first and third wells are completely isolated from the drain and source, and the substrate contact is located outside the first and third wells* (emphasis added).

That is, the Ker et al. I nowhere discloses either "the first and third wells are completely isolated from the drain and source" nor "the substrate contact is located outside the first and third wells." Therefore, the Kerr et al. I cannot overcome all of the deficiencies of the APAF.

Therefore, at least for the reasons above, it is respectfully submitted that neither the APAF nor Ker et al. I, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention and that claims 1, 7 and 13, and claims dependent thereon patentably distinguish thereover.

Claims 7, 8 and 10-12 were rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of Ker et al. II. Applicants respectfully traverse the rejection.

Claim 7 has been amended in a similar manner to claim 1. At least for the reasons discussed above for claim 1, the APAF also does not disclose all of the limitations of claim 7. In addition, the outstanding Office Action acknowledges deficiencies in the APAF and attempts to cure those deficiencies with Ker et al. II. However, Ker et al. II cannot overcome all of the deficiencies of the APAF as discussed below.

Ker et al. II discloses a substrate-triggered technique to effectively improve the ESD robustness of integrated circuit (IC) products. [16] In particular, Ker et al. II discloses a substrate-

[14] *Id.* at page 3, paragraph [0047], lines 17-18.
[15] *Id.* at page 3, paragraph [0047], lines 14-21.
[16] Ker et al. II at ABSTRACT.

triggered NMOS is positioned in a p-well **32** on a p-substrate **30**.[17] Two poly-silicon gates **34**, serving as the gate (electrode) of the substrate-triggered NMOS, are positioned above the p-well **32**.[18] Two n+ doped regions **36**, functioning as the drain (electrode) of the substrate-triggered NMOS, are positioned between poly-silicon gates **34** on the surface of the p-well **32**.[19] Between the n+ doped regions **36**, a p+ doped region **40** is positioned for the electrical connection to p-well **32** and serves as the trigger node for the substrate-triggered NMOS.[20] Isolation object(s) **42**, in this example, the silicon oxide formed by the shallow trench isolation processes, isolate the p+ doped region **40** from the n+ doped regions **36**.[21] The two n+ doped regions **38** on the surface(s) of p-well(s) 32 provide the source (electrode) of the substrate-triggered NMOS.[22] As shown in FIG. 5B, one of the n+ doped regions **38**, a p-well **32** and one of the n+ doped region 36 together can construct a parasitic npn bipolar junction transistor (BJT).[23]

In addition, Ker et al. II discloses an n-well **44** is positioned to partially overlay and electrically couple with the n+ doped region **38**.[24] Beside the n+ doped region **38**, a p+ doped region **46** forms the electrical connection to p-well **32'**.[25] All the surfaces of the p+ regions **46** and **40** are capped by silicide material.[26] The areas of the n+ doped regions **36** and **38** are patterned by a photo mask **52** to block silicide material on their surfaces but the contact areas will be still covered with silicide.[27]

Further, Ker et al. II discloses the contacts **54** for the n+ doped regions **36** must be separated from poly-silicon gate **34** by a specific distance, as shown in FIG. 5A, to sustain a higher ESD stress.[28] The shortest conductive path from the base of the npn BJT to the p+ doped

[17] *Id.* at column 1, lines 16-17.
[18] *Id.* at column 1, lines 17-20.
[19] *Id.* at column 1, lines 20-23.
[20] *Id.* at column 1, lines 23-25.
[21] *Id.* at column 1, lines 26-28.
[22] *Id.* at column 1, lines 28-31.
[23] *Id.* at column 1, lines 31-34.
[24] *Id.* at column 1, lines 35-36.
[25] *Id.* at column 1, lines 36-37.
[26] *Id.* at column 1, lines 37-39.
[27] *Id.* at column 1, lines 39-42.
[28] *Id.* at column 1, lines 43-45.

region **46** must travel around n-well **44**, to take advantage of the higher resistance provided by spread resistor Rsub.[29]

However, Ker et al. II nowhere discloses, as recited in independent claim 7:

> wherein a first, second and third wells are formed in a substrate of the triple well CMOS structure, a first well and third well of the triple well CMOS structure are completely isolated from a drain and source of the ESD NMOSFET, and the substrate contact is located outside the first and third wells.

That is, Ker et al. II cannot overcome all of the deficiencies of the APAF.

Therefore, at least for the reasons above, it is respectfully submitted that neither the APAF nor Ker et al. II, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention, and that claims 7, 8, 10 and 12, and claims dependent thereon patentably distinguish thereover.

Claim 9 was rejected under 35 U.S.C. 103(a) as unpatentable over APAF in view of Ker et al. II as applied to claim 7 above, and further in view of Ker et al. I. Applicants respectfully traverse the rejection.

Claim 9 is dependent on claim 7. Claim 7 has been amended in a similar manner to claim 1. Thus, at least for the reasons discussed above for claims 1 and 7, the APAF and Ker et al. II do not disclose all of the limitations of claim 9. In addition, the outstanding Office Action acknowledges deficiencies in the APAF and Ker et al. II and attempts to cure those deficiencies with Ker et al. I. However, Ker et al. I cannot overcome all of the deficiencies of the APAF and Ker et al. II, as discussed below.

[29] *Id.* at column 1, lines 45-49.

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However, neither Ker et al. I nor Ker et al. II discloses, as recited in independent claim 7:

> wherein a first, second and third wells are formed in a substrate of the triple well CMOS structure, a first well and third well of the triple well CMOS structure are completely isolated from a drain and source of the ESD NMOSFET, and the substrate contact is located outside the first and third wells.

However, Ker et al. II nowhere discloses, as recited in independent claim 7:

That is, neither Ker et al. I nor Ker et al. II can overcome all of the deficiencies of the APAF.

Therefore, at least for the reasons above, it is respectfully submitted that none of the APAF, Ker et al. I, and Ker et al. II, whether taken alone or in combination, disclose, suggest or make obvious the claimed invention, and that claim 9, and claims dependent thereon patentably distinguish thereover.

Conclusion

Based on the above amendments and arguments, Applicant respectfully submits that the application is in condition for allowance. If a fee is due, please charge Deposit Account No. 50-3223, under Order No. 21806-00156-US, from which the undersigned is authorized to draw.

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Respectfully submitted,

By Myron K. Wyche

Myron K. Wyche, Reg. No. 47,341
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorney for Applicant